REMARKS

Claims 1, 3-4 and 16-23 are all the claims presently being examined in the application. Claims 1, 3-4 and 16-23 stand rejected under 35 U.S.C. § 112, second paragraph. Claims 1, 3-4 and 16-23 also stand rejected on prior art grounds.

Applicant thanks the Examiner for the courteous and personal interview conducted on March 29, 2004, in which the Examiner agreed that the above claims would distinguish over the prior art of record. That is, Applicant has respectfully amended independent claims 1, 4 and 20, as indicated above and below, consistent with a proposal by Bradley Baumeister, Primary Examiner, as recorded in the Interview Summary of March 29, 2004. Accordingly, these amendments should overcome the rejections and place this case in condition for allowance.

With respect to the prior art rejections, claims 1, 3, 16, 17 and 21 stand rejected under 35 U.S.C. § 102(a) as being anticipated over the acknowledged prior art. Claims 4, 18, 19, and 22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kweon, et al. (U.S. Patent No. 5,834,832). Claims 20 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Degani, et al. (U.S. Patent No. 5,473,512).

These rejections are respectfully traversed in view of the following discussion.

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example by independent claim 1, is directed to a semiconductor device.

The semiconductor device includes a semiconductor chip, a chip-mounting substrate which is provided with the semiconductor chip mounted on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with the semiconductor chip electrically, solder balls formed on the first conductive pads, a printed circuit board on which second conductive pads connected with the solder balls are formed, and a solder mask formed on a bottom surface of the chip-mounting substrate. The solder mask includes a first uneven roughness, and underfill material is injected into a clearance formed between the chip-mounting substrate and the printed circuit board. The first uneven roughness is formed on a surface which is brought into contact with the underfill material. The first uneven roughness increases an area of a contact surface between the chip-mounting substrate and the underfill material. At least one of the first conductive pads and the second conductive pads includes a second uneven roughness. Importantly, the first uneven roughness and the second uneven roughness include substantially even spaced protrusions. (See Page 17, lines 10-13; and Figures 2-6, 9A and 9B).

Independent claim 4, is also directed to a semiconductor device. The semiconductor device includes a semiconductor chip, a lead frame which is provided with the semiconductor chip mounted thereon and electrically connected with the semiconductor chip, and a printed circuit board including conductive pads which are formed thereon and brought into direct contact with a bottom surface of the lead frame. The uneven roughness exists on the bottom surface of the lead frame and a surface of the conductive pads. Importantly, the uneven roughness includes substantially even spaced protrusions. (See Page 17, lines 10-13; and

Figures 2-6, 9A and 9B).

Independent claim 20, is also directed to a semiconductor device. The semiconductor device includes a semiconductor chip, a chip-mounting substrate which is provided with the semiconductor chip mounted on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with the semiconductor chip electrically, the chip-mounting substrate including Cu wirings, solder balls formed on the first conductive pads, a printed circuit board on which second conductive pads connected with the solder balls are formed, and material injected into a clearance formed between the chip-mounting substrate and the printed circuit board. A first uneven roughness is formed on a contact surface between the Cu wirings of the chip-mounting substrate and the solder balls. The first uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are directly connected to the solder balls to form a joined surface. The second conductive pad includes a second uneven roughness portion in contact with the solder balls. Importantly, the first uneven roughness and the second uneven roughness include substantially even spaced protrusions. (See Page 17, lines 10-13; and Figures 2-6, 9A and 9B).

As a result of this combination of features, the semiconductor device experiences less internal exfoliation of the components, and thus operates with a high level of reliability. (See Page 3, lines 15-21; Page 19, lines 22-24; and Page 22, lines 17-18).

II. The 35 U.S.C. § 112, Second Paragraph, Rejection

As indicated above, Applicant has amended independent claims 1, 4 and 20, consistent with the proposal by Bradley Baumeister, Primary Examiner, as recorded in the Interview Summary of March 29, 2004. In particular, Applicant has amended independent claims 1 and 20, to recite, " the first uneven roughness and the second uneven roughness

include substantially even spaced protrusions." Similarly, Applicant has amended independent claim 4 to recite, "the uneven roughness includes substantially even spaced protrusions."

Further, please note, the Applicant submits that the Examiner, for example, in a previous Office Action issued August 1, 2003, expressly admits that the Kweon, et al. reference (see above) does not disclose or suggest the "uneven roughness" feature, and thus this acknowledgment further supports Applicant's assertion that this rejection should not stand. (See Office Action, August 1, 2003, Page 6, Section 8).

In view of the foregoing, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REJECTIONS

As noted, the above claims are agreed to distinguish over the prior art of record. For the record, Applicant submits the following discussion.

A. The § 102(a) Rejection based on the Acknowledged Prior Art

Regarding claims 1, 3, 16, 17 and 21, the Acknowledged Prior Art ("Prior Art") fails to teach or suggest the features of independent claim 1, including the first uneven roughness and the second uneven roughness include substantially even spaced protrusions. (See Page 17, lines 10-13; and Figures 2-6, 9A and 9B).

The Interview Summary clearly indicates that the above feature distinguishes Applicant's invention over the prior art's flat surfaces as clearly shown in Figure 1 of the Specification. (See Interview Summary, March 29, 2004; and Application, Figure 1).

The Prior Art only pertains to semiconductor chips, which are attached to printed circuit boards, without an uneven roughness existing on either a bottom surface of a chip-

mounting substrate or a pad situated between the solder ball and the insulating substrate. Indeed, the Prior Art does not disclose, teach or suggest improving surface bonding. Accordingly, Applicant agrees with the Interview Summary, as indicated above, and the previous assertion in the Office Action of August 1, 2003, that the Prior Art is deficient and "does not disclose an uneven rough surface. " Thus, the Prior Art clearly does not teach or suggest that the first uneven roughness and the second uneven roughness include substantially even spaced protrusions as claimed by Applicant. Therefore, Applicant traverses the assertion in the Office Action that any "unevenroughness at the molecular scale" is structurally equivalent to a "surface roughness including substantially even spaced protrusions" as suggested. (See Application, Page 2, line 25-Page 3, line 21; Interview Summary, March 29, 2004; Office Action, August 1, 2003, Page 3-4, Section 5; and Office Action, March 1, 2004, Page 4).

As noted above, in Applicant's invention (e.g., as defined in Claim 1), the semiconductor device discloses including that the first uneven roughness and the second uneven roughness include substantially even spaced protrusions. In particular, "solder balls are connected with the Cu wirings by thermal compression, where the surface of the Cu wirings have been made roughened before hand." "[S]ince areas of jointed surfaces between the Cu wirings (the pads) and the solder balls increase because of unevennesses provided for the surfaces of the Cu wirings (the pads), the adhesive strength between the Cu wirings and the solder balls are heightened." Further, "[a]lthough unevennesses are provided for the pads formed on the chip-mounting substrate in the aforementioned embodiment, unevennesses may [be] provided for the pads formed on the printed circuit board as shown in FIG. 6A. Morever, as shown in FIG. 6B, unevennesses may be provided for the pads respectively formed on the chip-mounting substrate and the printed circuit board." (See Page 19, lines 1-

20; and Page 20, lines 3-10).

In contrast, as indicated above, the Prior Art does not include any uneven roughness, let alone, that the first uneven roughness and the second uneven roughness include substantially even spaced protrusions as disclosed in Applicant's invention.

Consequently, the Prior Art semiconductor device, which includes a printed circuit board and a semiconductor chip mounting substrate with an underfill material, is specifically directed to solving a problem of the different thermal expansion coefficients between the printed circuit board and the chip mounting substrate by providing for an underfill material to absorb a stress caused by these expansions. (See Page 1, line 22- Page 2, line 25). However, as discussed, the Prior Art devices without any uneven surface roughness have decreased reliability because a reduction occurs in the adhesive strength of an underfill material due to contamination or external mechanical stresses thus causing the underfill material to exfoliate from the chip-mounting substrate or the printed circuit board. (See Page 1, line 22 - Page 2, line 24; and Figure 1).

Thus, the Prior Art does not disclose, teach or suggest, including the first uneven roughness and the second uneven roughness include substantially even spaced protrusions as recited in claim 1, and related dependent claims 3, 16, 17 and 21.

B. The Kweon Reference

Regarding claims 4, 18, 19 and 22, Kweon, et al. ("Kweon") fails to teach or suggest the features of independent claim 4, including the uneven roughness includes substantially even spaced protrusions. (See Page 17, lines 10-13; Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-18; and Figures 9A and 9B).

The Interview Summary clearly indicates that the above feature distinguishes

Applicant's invention over the prior art's, i.e., Kweon, flat surfaces. (See Interview Summary, March 29, 2004). For the record, Applicant submits the following discussion.

Kweon only pertains to a packaging structure for a surface mounting type semiconductor package specifically directed to "improving the grounding property by the particular packaging structure, which allows a reduction of the noise, without deteriorating the operation speed or mounting density of the package." This purpose is achieved by providing "a nonconductive thin film as a capacitor formed in a space between the die pad 23 and the conductive pattern 32 where the space has a voltage difference." Accordingly, Kweon teaches that the die pad 23, the inner lead 25, the outer leads 27and the Vcc land patterns 29 include an even surface without an uneven roughness (See Kweon at Abstract; Column 1, lines 10-23; Column 3, lines 8-33; Column 4, line 25-Column 5, line 15; and Figures 1-7).

Based on this structural configuration, Applicant agrees with the Interview Summary, as indicated above, and the previous assertion in the Office Action of August 1, 2003, that Kweon is deficient, and does not "disclose the unevenroughness existing on the bottom surface of the lead frame and a surface of the conductive pads." Thus, Kweon clearly does not teach or suggest that the uneven roughness includes substantially even spaced protrusions as claimed by Applicant. Therefore, Applicant traverses the assertion in the Office Action that any "unevenroughness at the molecular scale" is structurally equivalent to a "surface roughness including substantially even spaced protrusions" as suggested. (See Application, Page 2, line 25-Page 3, line 21; Interview Summary, March 29, 2004; Office Action, August 1, 2003, Page 6, Section 8; and Office Action, March 1, 2004, Page 5; and Kweon at Abstract; Column 3, lines 14-43).

Thus, Kweon does not disclose, teach or suggest, including the uneven roughness

includes substantially even spaced protrusions as recited in claim 4, and related dependent claims 18, 19 and 22.

C. The § 103(a) Rejection of the Acknowledged Prior Art in view of Degani

Regarding claims 20 and 23, first, the references, separately, or in combination, fail to teach, disclose or provide a motivation for being combined.

Degani, et al. ("Degani") does not have the same aim as the Acknowledged Prior Art ("Prior Art"). Degani discloses a package for semiconductor electronic devices where the electronic device is held in place overlying a circuit board by at least three localized rigid support elements. Degani is specifically directed to alleviating the problems associated with "the mismatch of the thermal expansion coefficients" between the circuit board and the circuit chip of the electronic device. (See Degani at Abstract; Column 1, lines 15-20 and lines 55-62; and Column 2, lines 34-60).

Nothing within Degani, which focuses on relieving thermal stress between the circuit chip and the circuit board using at least three localized rigid support elements, has anything to do with underfill material for differences in thermal coefficients of expansion as disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with another invention, such as, Degani.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 20, including that the first uneven roughness and the second uneven roughness include substantially even spaced protrusions.

Degani does not make up for the deficiencies of the Prior Art, as discussed above.

Instead, Degani teaches that the circuit board 200 is attached to the mother board 100

through solder globules 201-204 situated intermediate between circuit board solder pads 221-224, which is sometimes coated with a solder masking layer 211, 216, and mother board wiring layers 101-104 coated with separate solder-stop layers 111-114. The solder pads 221-224 are situated on the underside of the circuit board 200 and the mother board wiring layers 101-104 are situated on the top surface of the mother board 100. The solder pads 221-224, and related solder masking layers 211, 216, as well as the wiring layers 101-104, and related solder-stop layers 111-114, have even surfaces without any uneven roughness. (See Degani at Abstract; Column 3, lines 40-55; Column 3, lines 8-33; and Column 6, lines 15-55; and Figures 1-3).

Based on this structural configuration, Applicant agrees with the Interview Summary, as indicated above, that Degani is deficient. Degani does not teach or suggest an uneven roughness on the solder pads 221-224, and related solder masking layers 211, 216, as well as the wiring layers 101-104, and related solder-stop layers 111-114, let alone, that an uneven roughness includes substantially even spaced protrusions as claimed by Applicant. Therefore, Applicant traverses the assertion in the Office Action that any "unevenroughness at the molecular scale" is structurally equivalent to a "surface roughness including substantially even spaced protrusions" as suggested. (See Application, Page 2, line 25-Page 3, line 21; Interview Summary, March 29, 2004; Office Action, March 1, 2004, Page 7; and Degani at Abstract; Column 2, lines 40-60).

Indeed, Degani does not teach or suggest Applicant's structure because Degani is focused on relieving thermal stress between the semiconductor chip and the mounting board. Therefore, Degani does not disclose, teach or suggest including that the first uneven roughness and the second uneven roughness include substantially even spaced protrusions. Thus, Applicant's invention provides for greater adhesive strength between the printed circuit

board and the solder balls when compared to Degani's structure.

For at least the reasons outlined above, Applicant respectfully submits that neither the Prior Art nor Degani disclose, teach or suggest all of the features of the independent claim 20, and related dependent claim 23.

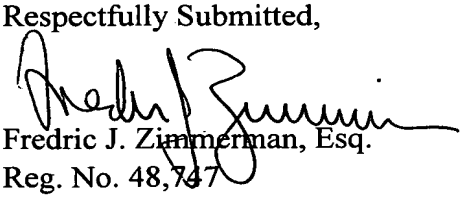
IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1, 3, 4, and 16-23, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,



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